

## Can NROM, a 2-bit, Trapping Storage NVM Cell, Give a Real Challenge to Floating Gate Cells?

Boaz Eitan<sup>(1)</sup>, Paolo Pavan<sup>(2)</sup>, Ilan Bloom<sup>(1)</sup>,  
Efraim Aloni<sup>(3)</sup>, Aviv Frommer<sup>(3)</sup>, David Finzi<sup>(3)</sup>

<sup>(1)</sup>Saifun Semiconductors, 65 Hamelacha st., Ind. Zone South, P.O.Box 8385, Netanya, 42504 Israel

Tel: 972-9-8850830 Fax: 972-9-8850831 e-mail: boaz@saifun.com

<sup>(2)</sup>Dipartimento di Scienze dell'Ingegneria e INFN, Università di Modena e Reggio Emilia,  
Via Campi 213/B, 41100 Modena, Italy

<sup>(3)</sup>Tower Semiconductors, P.O.Box 619, Migdal Haemeq, 23105 Israel

### Introduction

The NROM concept is a 2 bit Flash cell based on charge storage in ONO dielectric. The cell is storing two physically separated bits with a unique method to sense the trapped charge. Programming is performed by Channel Hot Electron injection (CHE) and erase by Hot Hole Enhanced Tunneling (HHET).

For a new technology to challenge the 30 years old Floating Gate cells, the total solution from Cell, Array, Process, Product and Testing has to be available. To actually "challenge" Floating Gate as the main Flash technology, a technology has to be in volume production. NROM technology is in initial production stage, hence we can only discuss future potential to become a true challenge to the Floating Gate storage concept.

In this presentation, we will introduce the NROM technology. The NROM technology is compared to the Floating gate Flash.

### The NROM Cell and Array

The NROM cell is an n-channel MOSFET device where the gate dielectric is replaced with a trapping material (Nitride) sandwiched between two silicon dioxide layers (ONO, Fig. 1) [1-4]. The top and bottom oxides are thicker than 50Å to avoid any direct tunneling. The charge is stored in the nitride next to the  $n^+$  junctions.

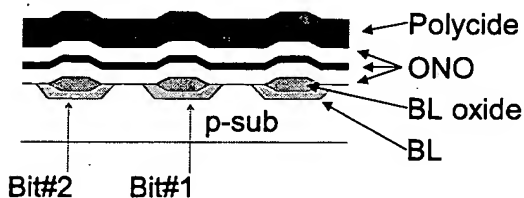


Fig. 1. The NROM cell: cross section along a Word Line.

To add the NROM Flash block to a standard CMOS process, the ONO layer is added after the field isolation and before the gate oxidation. For a virtual ground array, there are 2 extra masking steps to generate the array and 2 more, for the high voltage transistors. The NROM module hardly affects any of the CMOS thermal

budgets. This is a very simple process, with great potential for embedded applications.

The virtual ground array is a fieldless crosspoint architecture (Fig. 2) with  $5-6F^2$  cell size or  $2.5-3F^2$  per bit. In a  $.35\mu$  technology, cell area is  $.315\mu^2$  per bit and  $.2\mu^2$  in  $.25\mu$  technology. This small cell size is purely the result of the lithography and minimum Leff limitations. No coupling considerations like in the floating gate technology add to cell size, since coupling is 1 in this concept.

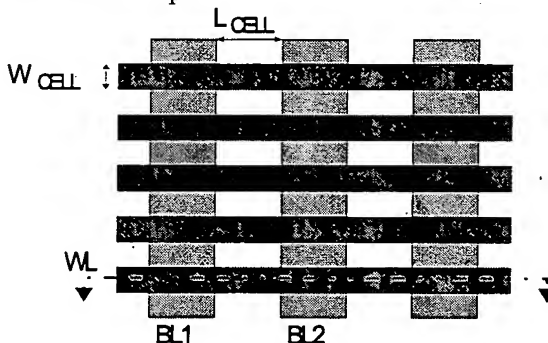


Fig. 2. A schematic of the Virtual Ground array.

### Operation principles and experimental results

The NROM cell is programmed by CHE, for example, using Figs. 1 and 2 as a reference, to program Bit#1,  $V_{BL1}=0$ ,  $V_{BL2}=4.5V$  and  $V_{WL}=9V$ . Electrons are injected and trapped, next to junction BL2. To maximize the sensitivity of the read operation, the stored charge is sensed, next to the source terminal. Low  $V_{WL}$  is applied to further enhance the read sensitivity, by minimizing the potential drop across the trapped charge. Bit #1 is read by applying 1.5V to BL1, 0V to BL2 and  $V_{WL}$  of  $\sim 3V$ , we call it "reverse read", since the read and programming source and drain terminals are interchanged. The 2<sup>nd</sup> bit is programmed and read by reversing the terminals in both operations. The two-bit programming is shown in Fig. 3. The reason one bit does not affect the information of the other bit, is the narrow trapped charge region ( $\sim 100\text{\AA}$  wide). It permits to "read through" the trapped charge region, even at this low BL voltage (1.5V).

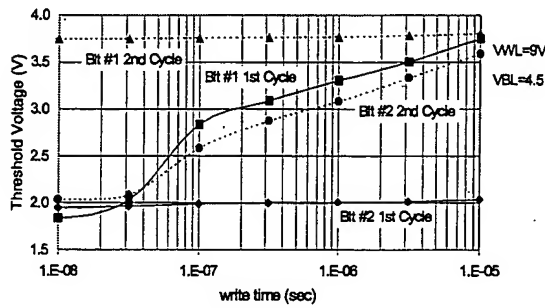


Fig. 3. Programming results for two bit operation. In 1<sup>st</sup> cycle only Bit#1 is programmed and Bit#2 is remaining erased. In the 2<sup>nd</sup> cycle only Bit#2 is programmed and Bit#1 stays programmed.

The erase involves hole injection through the bottom oxide. The holes are generated by band to band tunneling; they are accelerated by the lateral field and are injected through the bottom oxide. The injection probability is strongly dependent on the vertical field. A typical set of erase characteristics is shown in Fig. 4. The BL potential is affecting both the lateral and vertical fields; hence the erase is more sensitive to it.

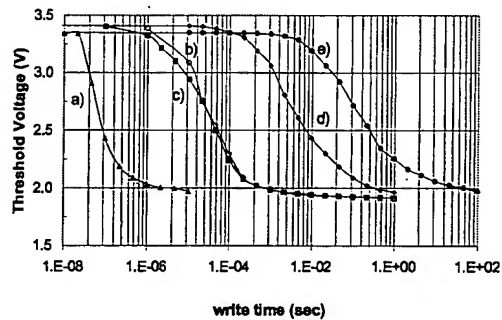


Fig. 4. Erase results with the BL and WL voltages as a parameter. The erase conditions are: a)  $V_{BL}/V_{WL}/V_{SL} = 7/-3/3$ , b)  $8/0/3V$ , c)  $5/-5/0$ , d)  $3/-10/0$ , e)  $3/-7/0$ .

Erase can be performed with positive voltage only, positive  $V_{BL}$  and zero on the gate. This is very attractive to eliminate the extra process and area, required for negative gate voltage during erase.

#### Reliability, Retention and Endurance

The very special effect of the localized trapping, is the high reliability associated with it. No dielectric defect can cause the loss of the entire charge. The charge transfer is between every trap and the Si. Very little [2] lateral charge movement has been observed. The localized erase eliminates the over erase problem.

High temperature retention results are shown for both the high and low  $V_T$  states. The total change in  $V_T$  after 1,700Hrs at 250°C, is less than .4V (Fig. 5). This is the first time the retention of charge trapping device has achieved the same results as the Floating Gate device [5-7]. It stems from the relatively thick bottom and top oxides, with a nitride stabilization process step.

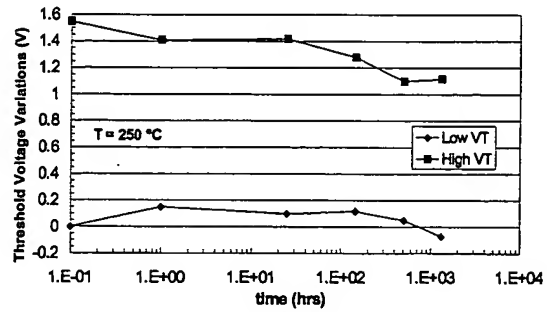


Fig. 5. Retention results at 250 °C for 1,700 hours.

The endurance of the NROM concept up to 1M cycles depends on the programming control. A typical result is shown in Fig. 6. No true degradation mechanism is detected since a cycle involves only ~200-500 electron exchange, a factor of ~100 lower than floating gate devices. Another advantage is in the fact that both erase and programming involve hot carriers, hence the injection is at relatively low oxide fields. The product and single cell show identical results. There are no issues related to  $V_T$  distribution, like faster degradation or "erratic" behavior.

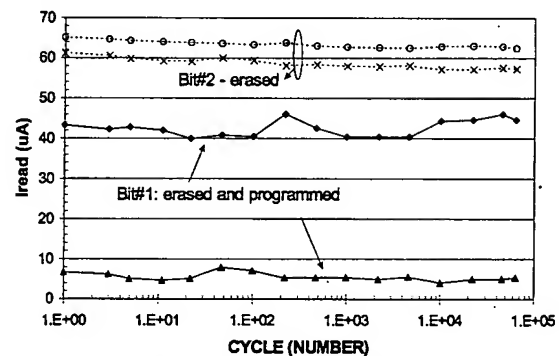


Fig. 6. Cycling results only Bit#1 is cycled, Bit#2 unaffected. Program conditions are  $V_{BL1} = 4.5V$ ,  $V_{WL} = 9V$ ,  $t_p = 2\mu s$ . Erase conditions are:  $V_{BL1} = 7V$ ,  $V_{WL} = 0V$ ,  $t_e = 100ms$ . Erase is up to 60% of the initial  $I_{READ}$ .

#### Comparison to Floating Gate Devices

In this presentation a comparison of two technologies, NROM and Floating Gate, is discussed. This comparison helps in understanding the NROM cell and technology.

Table 1 is an attempt to point out the key parameters to compare the two concepts from the cell up to the product level.

**Table 1**

Parameter	Floating Gate	NROM	Comment
Bit Size	6-10F <sup>2</sup>	2.5 F <sup>2</sup>	
Die Size	1X	.4X	Same Design Rules
Process steps	CMOS +~10-12 Masks	CMOS +~4 Masks	
Process Complexity	Very Complex	Simple	
Integration with CMOS, for Embedded Applications	Very Complex	Simple	
WL delay	4X (A.U.)	<1X (A.U.)	2 Bit cell =4X RC reduction
Design Complexity	High	High	
Erase V <sub>t</sub> Distribution	.5-2.5V	1.3-1.8V	
Over Erase	Severe problem	No issue	
Low Voltage Application	Difficult	Less Difficult	
Charge per cycle	~10K Electrons	~200-500 Electrons	
Maturity	Very High	New	

This comparison shows the great advantages in all aspects of the flash applications. Smaller cell size results in a smaller die size. Substantially simpler process leads to a better fit to embedded flash. The smaller erased V<sub>T</sub> window improves the low voltage product implementation.

In conclusion, we have introduced a new Flash concept, NROM, based on a 2 bit localized trapping concept. This technology is a paradigm change in NVM, it can replace all Floating Gate devices, EPROM, Flash and EEPROM with their NROM version.

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